REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-11, 13-16 and 18 are present in this application, claims 12 and 17 being cancelled by way of the present amendment. Claims 1, 2 and 12-18 are rejected under 35 U.S.C. § 102(e) over U.S. 6,847,388 Anderson. Claims 3-11 are withdrawn from consideration.

The present invention is directed to an image processing apparatus. The image processing apparatus has an image processing part which includes a buffer memory for data storage, and image processing unit which writes image data to the buffer memory, and a compression unit for compressing the image data read from the buffer memory. The buffer memory is connected to receive only the image data from the image processing unit and output the image data only to the compression unit. With such a configuration, the image processing apparatus can process data more efficiently.

Anderson describes a method and system for accelerating a user interface of an image capture unit. Referring to Figure 7, raw image data from image device 114 is input to input buffers 538. Data is output from input buffers 538 to Live View Generation unit 612 and RAM Spoolers 620. Unit 612 produces data in the YCC 222 format which is stored in frame buffers 536. Frame buffers 536 output the YCC 222 data to LCD 402 and Conversion and Compression unit 614. This is described beginning at column 8, line 59 and continuing to column 9, line 41.

Input buffers 538 and frame buffers 536 have the structure shown in Figure 4B, each having buffers A and B, which is described as a "ping-pong" arrangement (see column 5, lines 65-column 6, line 14). As is clear from Figure 7 and the description in the specification, Anderson uses input buffers 538 to output data to both unit 612 and RAM Spoolers 620, and

uses frame buffers 536 to output data to LCD 402, unit 614 and Conversion and Resizing unit 616.

The system of Anderson et al. does not disclose or suggest the image processing apparatus of claim 1. The apparatus of claim 1 includes a buffer memory for data storage an image processing unit for performing a predetermined process on the capture data, and a compression unit for compressing the image data read from the buffer memory. The buffer memory is connected to receive only the image data from the image processing unit and connected to output the image data only to the compression unit. Such a structure is shown in the non-limiting example of Figures 1 and 2 of the present specification, where local buffers A and B are connected between Real Time Processing unit 7 and Image Compression and Expansion unit 13.

As the frame buffers 536 in Anderson are not connected to output the image data only to the compression unit 612, where instead data is output to LCD 402 and units 614 and 616, and the input buffers 538 output data to both unit 612 and spooler 620, there is clearly no suggestion of claim 1 in Anderson. Withdrawal of the rejection of claim 1 based upon Anderson is respectfully requested.

The apparatus of Claim 15 includes first and second buffer memories connected in parallel for data storage, where the first and second buffer memories are connected to receive only image data from the image processing unit and connected to output the image data only to the compression unit. As is apparent from the above discussion of Anderson, there is no such apparatus disclosed or suggested in Anderson since frame buffers 536 output data to LCD 402 and units 614 and 616, and input buffers 538 output data to both unit 612 and spooler 620. Claim 15 is also patentably distinguishable over Anderson, and withdrawal of the rejection of claim 15 based upon Anderson is respectfully requested.

It is respectfully submitted the present application is in condition for allowance, and the favorable action to that effect is respectfully requested.

Respectfully submitted,

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